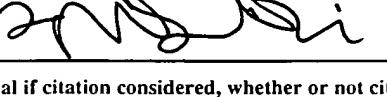


<b>INFORMATION DISCLOSURE CITATION</b> <i>(Use several sheets if necessary)</i>				Docket Number (Optional) <b>FIS9-2001-039</b>		Application Number <b>10/040,122</b>	
				Applicant(s) <b>SCOTT ET AL.</b>		Filing Date <b>01/02/02</b>	
<b>U.S. PATENT DOCUMENTS</b>							
*EXAMINER INITIAL	REF	DOCUMENT NUMBER	DATE	NAME	CLASS	SUBCLASS	FILING DATE IF APPROPRIATE
WD		6,256,759	07-03-01	BHAWMIK ET AL.			
WD		5,737,340	04-07-98	TAMARAPALLI ET AL.			
WD		6,070,261	05-30-00	TAMARAPALLI ET AL.			
WD		6,038,691	03-14-00	NAKAO ET AL.			
WD		5,828,828	10-27-98	LIN ET AL.			
<b>FOREIGN PATENT DOCUMENTS</b>							
REF	DOCUMENT NUMBER	DATE	COUNTRY	CLASS	SUBCLASS	Translation	
						YES	NO
<b>OTHER DOCUMENTS</b> <i>(Including Author, Title, Date, Pertinent Pages, Etc.)</i>							
WD		"TEST POINT INSERTION FOR SCAN-BASED BIST" SEISS ET AL. PROCEEDING OF THE EUROPEAN TEST CONFERENCE, pp. 253, 1991.					
WD		"TESTABILITY-DRIVEN RANDOM TEST-PATTERN GENERATION" LISANKE ET AL., IEEE TRANSACTIONS ON COMPUTER-AIDED DESIGN, Vol. CAD-6, Nov. 1987, pp. 1082-1087.					
WD		"ON TESTABILITY ANALYSIS OF COMBINATIONAL NETWORKS" BRGLEZ ET AL, PROCEEDINGS OF INTERNATIONS SYMPOSIUM ON CIRCUITS AND SYSTEMS, pp.221-225, 1984.					
WD		"ON GENERATING OPTIMAL SIGNAL PROBABILITIES FOR RANDOM TESTS: A GENETIC APPROACH", SRINIVAS ET AL. VLSI DESIGN, 1996, VOL. 4, NO. 3, pp 207-215.					
WD		"STATISTICAL FAULT ANALYSIS", JAIN ET AL. IEEE DESIGN & TEST OF COMPUTERS, VOL. 2, NO.2 pp. 38-44.					
EXAMINER				DATE CONSIDERED <b>9/2003</b>			
<b>EXAMINER:</b> Initial if citation considered, whether or not citation is in conformance with MPEP Section 609; Draw line through citation if not in conformance and not considered. Include copy of this form with next communication to applicant.							

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